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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 1400.4100276

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on 09/05/2006
Signature: /Ross D. Snyder/
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Application Number	Filed
09/636,115	08-10-2000

First Named Inventor: Adrian Grah, et al.

Art Unit	Examiner
2115	Cao, Chun

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☒ attorney or agent of record. Registration number 37,730
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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09/05/2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Adrian Grah, et al.

Title: METHOD AND APPARATUS FOR CONTROLLING A CLOCK SIGNAL OF A LINE CARD CIRCUIT

App. No.: 09/636,115 Filed: 08-10-2000

Examiner: Cao, Chun Group Art Unit: 2115

Atty. Dkt. No. 1400.4100276

Mail Stop AF
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Claims 1-19 are pending in the present application. Claims 6-10 and 16-19 are withdrawn from consideration. The Examiner has rejected claims 1-5 and 11-15. Applicant respectfully requests reconsideration of pending claims 1-5 and 11-15. Applicant files herewith a notice of appeal. Pursuant to the "New Pre-Appeal Brief Conference Pilot Program," 1296 Off. Gaz. Pat. Office 67 (July 12, 2005) and the "Extension of the Pilot Pre-Appeal Brief Conference Program" dated 1/10/2006, Applicant submits a pre-appeal brief request for review. The review is requested for the reasons set forth below:

Applicant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection. Applicant submits the Examiner's "Response to Arguments" provides evidence that the Examiner has failed to consider the pending claims as required by the Manual of Patent Examining Procedure (MPEP) and prevailing case law. For anticipation under 35 U.S.C. § 102, a reference must teach every aspect of the claimed invention either explicitly or implicitly. Any feature not directly taught must be inherently present [emphasis added]. See MPEP 706.02 – distinction between 35 U.S.C. § 102 and § 103. As Applicant describes in detail below, Applicant submits there exist clear errors in the Examiner's rejections and/or the Examiner's omissions of one or more essential elements needed for a *prima facie* rejection.

The Examiner has rejected claims 1-5 and 11-15 under 35 U.S.C. § 102(b) as being anticipated by Oki (U.S. Patent No. 5,870,595). Applicant respectfully disagrees. Regarding claim 1, the Examiner cites "[61, fig. 2; col. 5, lines 8-25]" as allegedly disclosing "an activity latch" and "[the size of the available area; col. 5, lines

8-25]" as allegedly disclosing "for holding an activity flag value." Applicant submits the cited portion of the cited reference fails to disclose the subject matter set forth in claim 1, for example, "an activity latch for holding an activity flag value." While the Examiner alleges "third buffer memory unit" 61 of Oki to disclose "an activity latch" and "[the size of the available area; col. 5, lines 8-25]" to disclose "for holding an activity flag value," Applicant notes that "third buffer memory unit" 61 is depicted as providing only one output, namely reference numeral 72, which is recited as "outgoing data" (col. 5, lines 16 and 17). Applicant can find no teaching in the cited portion of the cited reference that AND circuit 83, which the Examiner alleges as disclosing "a logic element operatively coupled to the activity latch to receive an incoming clock signal and to provide an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value," provides an outgoing clock signal, the outgoing clock signal being dependent on the activity flag value. Moreover, while the Examiner asserts "[the size of the available area]" as allegedly disclosing "an activity flag value," Applicant can find no teaching in the cited portion of the cited reference of "third buffer memory unit 61" holding "the size of the available area" as "an activity flag value." Applicant notes the Examiner again cites, "[figures 1 and 2; col. 4, line 58-col. 5, line 29; emphasis added, 'signal 54 is generated based on an value detected by detecting unit 66 from buffer memory 61 (see col. 5, lines 8-12), and output to an AND logic circuit 83 to control an output (clock signal 80) of a clock signal 6 (see fig. 1; col. 5, lines 22-29)']." As Applicant noted in Applicant's response to the previous Office action, Applicant has exhaustively searched the entire Oki reference and is unable to locate such text as purportedly quoted by the Examiner. While the Examiner cites col. 5, lines 8-12, that portion of the cited reference does not appear to contain the text purportedly quoted by the Examiner. Rather, col. 5, lines 8-12, states, "Reference numeral 68 is a comparator which is used for generalizing the second transfer halt signal 54 cited above when the size of the available area in the first buffer memory unit 66 is smaller than a predetermined value." Applicant notes the only mention of "value" in the cited portion of the cited reference is "a predetermined value." Applicant can find no teaching in the cited portion of the cited reference of the "predetermined value" being "an activity flag value" or of "an activity latch for holding" the "predetermined value."

Regarding claim 2, for example, the Examiner asserts AND gates 81a and 81b of Figure 8 of Oki as allegedly disclosing "a second activity latch" of claim 2. Applicant can find no teaching in the cited portion of the cited reference of AND gates 81a or 81b holding a second activity flag value. Moreover, as AND gates are purely combinational logic gates, Applicant submits the AND gates cited by the Examiner fail to disclose a second activity flag value held in a second activity latch. Furthermore, Applicant can find no teaching in the cited portion of the cited reference of "wherein the activity flag value is mutually exclusive with a second activity flag value.

Regarding claim 3, for example, Applicant submits the cited portion of the cited reference fails to disclose that the logic element passes the incoming clock signal as the outgoing clock signal when the activity

flag value has a first value. As Applicant has argued Oki's absence of "an activity latch for holding an activity flag value," Applicant submits Oki fails to disclose an "activity flag value" consonant with the subject matter of claim 3. While the Examiner cites col. 5, lines 25-29, and col. 11, lines 34-37, as allegedly disclosing the subject matter of claim 3, Applicant can find no teaching as to "when the activity flag has a first value" in the cited portions of the cited reference.

Regarding claim 4, for example, Applicant submits the cited portion of the cited reference fails to disclose that the logic element blocks the incoming clock signal when the activity flag value has a second value. As Applicant has argued Oki's absence of "an activity latch for holding an activity flag value," Applicant submits Oki fails to disclose an "activity flag value" consonant with the subject matter of claim 4. While the Examiner cites col. 5, lines 25-29, and col. 11, lines 34-37, as allegedly disclosing the subject matter of claim 4, Applicant can find no teaching as to "when the activity flag has a second value" in the cited portions of the cited reference.

Regarding claim 5, for example, Applicant submits the cited portion of the cited reference fails to disclose that the logic element provides a static output level as the output clock signal when the activity flag value has the second value. As Applicant has argued Oki's absence of "an activity latch for holding an activity flag value," Applicant submits Oki fails to disclose an "activity flag value" consonant with the subject matter of claim 5. While the Examiner cites col. 5, lines 25-29; col. 11, lines 34-37; col. 11, lines 38-47; and col. 12, lines 14-21, as allegedly disclosing the subject matter of claim 5, Applicant can find no teaching as to "when the activity flag has a second value" in the cited portions of the cited reference.

Regarding claims 11-15, the Examiner alleges claims 11-15 are basically the operating step that are carried out by the corresponding elements in claims 1-5 and rejects claims 11-15 for the same reason set forth for claims 1-5. However, Applicant submits claim limitations of claims 1-5 cannot be imputed to claims 11-15, as claims 11-15 do not depend from any of claims 1-5. As to claim 11, Applicant submits Oki fails to disclose a "receiving a first activity flag value from a first activity latch of a first line card circuit of the plurality of line card circuits" as set forth in claim 11. As to claim 12, Applicant submits Oki fails to disclose either a "first activity latch" or a "second activity latch." Moreover, Applicant notes that none of the teachings of Oki, column 11, lines 56-61, cited by the Examiner appear to disclose the feature of claim 12 "the second activity flag value being mutually exclusive of the first activity flag value." Thus, Applicant submits that claim 12 is in condition for allowance. Regarding claims 13-15, as noted above, Applicant submits Oki fails to disclose the features of claim 11 from which claims 13-15 depend. Moreover, Applicant submits Oki fails to disclose a "first activity flag value" consonant with the subject matter of claims 13-15.

The Examiner has rejected claims 1, 3-5, 11, and 13-15 under 35 U.S.C. § 102(b) as being anticipated by Karibe et al. (Karibe), JP Patent No. 64-48142. In section 8 of the Office action, the Examiner states,

"Karibe discloses an activity latch of a line card [fig. 2] for holding an activity flag value [counter 5; abstract all]." Applicant respectfully disagrees. Regarding claim 1, the Examiner alleges that counter 5 of Figure 1 of Karibe discloses "an activity latch for holding an activity flag value." However, Applicant submits that counter 5 of Karibe's "Address Compare Stop Control System" fails to disclose "an activity latch" of a "line card circuit," as set forth in claim 1. Thus, Applicant submits that Karibe fails to disclose the subject matter of claim 1.

Regarding claim 3, the Examiner alleges that Karibe discloses the logic element passes the incoming clock signal as the outgoing clock signal when the activity flag value has a first value. The Examiner purports to quote Karibe as stating, "has a not ZERO value," but Applicant is unable to locate such text in Karibe. Thus, Applicant submits that Karibe fails to disclose the teaching attributed by the Examiner.

Regarding claim 4, the Examiner alleges that Karibe discloses the logic element blocks the incoming clock signal when the activity flag value has a second value. The Examiner purports to quote Karibe as stating, "has a ZERO value," but Applicant is unable to locate such text in Karibe. Thus, Applicant submits that Karibe fails to disclose the teaching attributed by the Examiner.

Regarding claim 5, the Examiner alleges that Karibe inherently discloses the logic element provides a static output level as the output clock signal when the activity flag value has the second value. While the Examiner asserts a rejection based on inherency, Applicant submits the Examiner has not complied with MPEP § 2112 (Requirements of Rejection Based on Inherency). For example, Applicant submits that the Examiner has not provided a rationale or evidence tending to show inherency, pursuant to MPEP § 2112 IV.

Furthermore, Applicant submits that the teachings of the cited reference fail to establish inherency in accordance with existing law. For example, Applicant submits that the Examiner has failed to establish that the public gained the benefit of the subject matter recited in claim 5 from the teachings of the cited reference. *Schering Corp. v. Geneva Pharmaceuticals*, 339 F.3d 1373 (Fed. Cir. 2003). As another example, Applicant submits that the Examiner has failed to establish that the subject matter recited in claim 5 is present in the teachings of the cited reference. *Mentor v. Medical Device Alliance*, 244 F.3d 1365 (Fed. Cir. 2001); *Scaltech v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999). Thus, Applicant submits that the subject matter recited in claim 5 cannot be considered to be inherent in the teachings of the cited reference. Therefore, Applicant submits that the Examiner has not shown claim 5 to be anticipated by the cited reference.

Regarding claims 11 and 13-15, the Examiner states, "As to claims 11 and 13-15 basically are the operating step that are carried out by the corresponding elements in claims 1 and 3-5." Accordingly, claims 11 and 13-15 are rejected for the same reason as set forth for claims 1 and 3-5." Applicant has presented above arguments as to why claims 1 and 3-5 are allowable. As the Examiner does not raise any other bases for

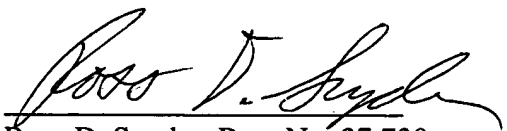
rejection of claims 11 and 13-15 besides those raised with respect to claims 1 and 3-5, Applicant reiterates Applicant's above arguments to whatever extent they may be applicable to claims 11 and 13-15. However, Applicant submits claim limitations of claims 1 and 3-5 cannot be imputed to claims 11 and13-15, as claims 11 and 13-15 do not depend from any of claims 1 and 3-5. Regarding claim 11, Applicant can find no teaching in the cited portion of the cited reference of "...a first activity latch of a first line card of the plurality of line cards." Regarding claim 13-15, as Applicant has presented arguments that the cited portion of the cited reference fails to disclose the features of claim 11, from which claims 13-15 depend, Applicant submits the cited portion of the cited reference fails to disclose features consonant with the subject matter recited in claims 13-15.

The Examiner has rejected claims 1 and 11 under 35 U.S.C. 102(b) as being anticipated by Senoh, U.S. Patent No. 5,914,580. Applicant respectfully disagrees. Regarding claim 1, for example, Applicant submits the cited portion of the cited reference fails to disclose "an activity latch for holding an activity flag value." While the Examiner cites "[10, fig. 2]" and "[col. 4, lines 45-53]," Applicant can find no teaching in the cited portions of the cited reference of "an activity latch for holding an activity flag value." Also, Applicant notes the subject matter of claim 1 is directed to a "line card circuit." Applicant can find no teaching in the cited portion of the cited reference of a "line card circuit."

Regarding claim 11, for example, Applicant submits the cited portion of the cited reference fails to disclose "receiving a first activity flag value from a first activity latch of a first line card circuit of the plurality of line card circuits." The Examiner states "claim 11 is rejected for the same reasons as set forth for claim 1." For the rejection of claim 1, the Examiner cites "[10, fig. 2]" and "[col. 4, lines 45-53]." Applicant can find no teaching in the cited portions of the cited reference of "...a first activity latch of a first line card of the plurality of line cards." Applicant submits the cited reference appears to be directed to a drive control device for a stepping motor, not a first line card circuit of a plurality of line card circuits.

Respectfully submitted,

09/05/2006
Date



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